Analog Power

AM30N02-40D

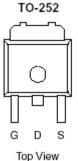
N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low r_{DS(on)} Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY				
V _{DS} (V)	r _{DS(on)} m(Ω)	I _D (A)		
20	$29 @ V_{GS} = 4.5V$	34		
	$43 @ V_{GS} = 2.5V$	22		





Parameter			Limit	Units
Drain-Source Voltage		V _{DS}	20	v
Gate-Source Voltage		V _{GS}	±12	v
Continuous Drain Current ^a	$T_C=25^{\circ}C$	I _D	34	•
Pulsed Drain Current ^b		I _{DM}	40	A
Continuous Source Current (Diode Conduction) ^a		Is	30	Α
Power Dissipation ^a	$T_{\rm C}=25^{\rm o}{\rm C}$	P _D	50.0	W
Operating Junction and Storage Temperature Range	•	T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	°C/W	
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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Parameter	Symbol	Same Lal Tract Constitutions	Limits			TT:4	
rarameter	Symbol Test Conditions		Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$	0.7			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{pq} = 16 V V_{cq} = 0 V$			1	uA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			25	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 4.5 V$	34			Α	
Drain-Source On-Resistance ^A		$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$			29	mΩ	
Drain-Source On-Resistance	r _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 11 \text{ A}$			43		
Forward Tranconductance ^A	g _{fs}	$V_{DS} = 10 \text{ V}, I_D = 17 \text{ A}$		22		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S} = 34$ A, $V_{\rm GS} = 0$ V		1.1		V	
Dynamic ^b							
Total Gate Charge	Qg	$\mathbf{X} = 10 \mathbf{X} \mathbf{X} = 45 \mathbf{X}$		13.4			
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 11 \text{ A}$		0.9		nC	
Gate-Drain Charge	Q _{gd}	$I_D = 11$ A		2.0		1	
Turn-On Delay Time	t _{d(on)}			16			
Rise Time	t _r	V_{DD} = 10 V, R_L = 25 Ω , I_D = 34 A,		5		nS	
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 V$		23		115	
Fall-Time	t _f			3			

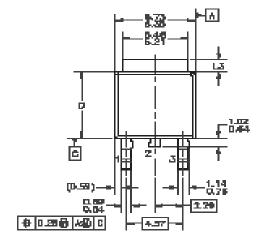
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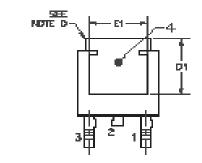
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

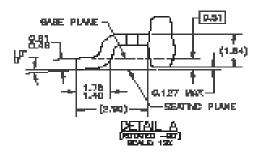
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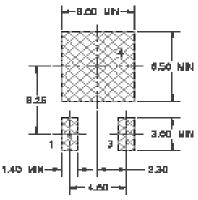
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Package Information

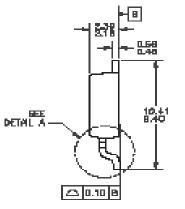








LAND PATTERN RECOMMENDATION



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